ABSTRACT OF THE DISCLOSURE

The present invention provides a semiconductor inspection method which detects a short circuit failure of adjacent lines having the possibility of a short circuit occurring, which short circuit failure cannot be detected by the conventional semiconductor inspection methods. The semiconductor inspection method comprises steps of: extracting adjacent lines having the possibility of a short circuit occurring between the lines from a layout patter of a semiconductor (step S101), obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0" (step S102), and monitoring outputs of a logical circuit which receives the input logical values, thereby to compare the outputs with output logical values which are expected when the input logical values are input to the logical circuit (step S103). Therefore, the short circuit failure of the adjacent lines in the logical circuit can be correctly detected in a short time.